

ABSTRACT OF THE DISCLOSURE

Sub
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5 A data processing system with a microprocessor (10). The microprocessor has in instruction execution pipeline that includes fetch and decode stages and several functional execution units (L1/2, S1/2, M1/2, D1/2). Fetch packets contain a plurality of instruction words. Execution packets include a plurality of instruction words that can be executed in parallel by two or more execution units. An execution packet can span two or more fetch packets. An add (k)constant to program counter (ADDKPC) instruction is provided, such that a parameter specified by the ADDKPC instruction is combined with a value provided by a program counter of microprocessor. The ADDKPC instruction can also specify a number of delay slots after a branch instruction to be filled with virtual NOP instructions such that memory is not wasted with useless NOP instructions. An ADDKPC instruction can provide a relative address for use as a return address. A plurality of predicated ADDKPC instruction can provide a return address selected from a plurality of return address. A compiler can reorder code with an ADDKPC instruction to absorb useless NOP instructions.

Figure 9